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73 L1

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L1

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L4L3 710/100,305,52,72;377/41;326/21,52,62;365/189.01,189.07.ccls.

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DB=PGPB,USPT,USOC; PLUR=YES; OP=OR

L1 invert\$4 same data same (mask\$3 near5 (pin or terminal))

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2	<input type="checkbox"/>	<input type="checkbox"/>	US 6671212 B2	20031230	13	Method and apparatus for data inversion in memory	365/189.07	365/189.04	
3	<input type="checkbox"/>	<input type="checkbox"/>	US 5495190 A	19960227	11	Arbiter circuit	327/19	327/18; 327/23;	
4	<input type="checkbox"/>	<input type="checkbox"/>	US 4727363 A	19880223	14	Video ram write control apparatus	345/563	345/531	
5	<input type="checkbox"/>	<input type="checkbox"/>	US 4580100 A	19860401	24	Phase locked loop clock recovery circuit for data	360/51	329/314; 331/1A;	
6	<input type="checkbox"/>	<input type="checkbox"/>	US 3617134 A	19711102	7	OPTICAL IMAGE FRAME COORDINATE DATA DETERMINING	356/141.3	250/237G; 352/236;	

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Integrated detectors for embedded optical interconnections on electrical boards, modules, and integrated circuits

[Sang-Yeon Cho](#) [Sang-Woo Seo](#) [Brooke, M.A.](#) [Jokerst, N.M.](#)

Nat. Sci. Found. Packaging Res. Center, Georgia Inst. of Technol., Atlanta, GA

 This paper appears in: **Selected Topics in Quantum Electronics, IEEE J u**

Publication Date: Nov.-Dec. 2002

On page(s): 1427 - 1434

Volume: 8 , Issue: 6

ISSN: 1077-260X

Inspec Accession Number: 7517919

Abstract:

Significant opportunities exist for optical interconnections at the board, module level if compact, low-loss, high-data-rate optical interconnections can be integrated into these electrical interconnection systems. To create such an integrated optoelectronic/electronic microsystem, **mask**-based alignment of the optical interconnection waveguide, optoelectronic active devices, and interface circuitry is attractive from a packaging alignment standpoint. This paper describes an integrated process for creating optical interconnections which can be integrated in a post-format onto standard boards, modules, and integrated circuits. These optical interconnections utilize active thin-film optoelectronic components embedded in a waveguide/interconnection substrate, thus eliminating the need for optical beam elements and their alignment, and providing an electrical output on the substrate. An optical interconnection. These embedded optical interconnections are reproduced using BCB polymer optical waveguides with embedded InGaAs-based thin-film metal-semiconductor-metal (I-MSM) photodetectors on an Si substrate. These interconnections have been fabricated and tested, and the coupled optical signal was supported by an experimental estimate of 47.8%. The measured full-width maximum of the electrical pulse from the MSM photodetector embedded in the waveguide was 16.73 ps for an input 500-fs optical laser pulse.

Index Terms:

[III-V semiconductors](#) [gallium arsenide](#) [indium compounds](#) [integrated circuit packaging](#) [optoelectronics](#) [metal-semiconductor-metal structures](#) [optical films](#) [optical interconnections](#)

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File: PGPB

Aug 21, 2003

PGPUB-DOCUMENT-NUMBER: 20030158981
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20030158981 A1

TITLE: Memory bus polarity indicator system and method for reducing the affects of simultaneous switching outputs (SSO) on memory bus timing

PUBLICATION-DATE: August 21, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
LaBerge, Paul A.	Shoreview	MN	US	

APPL-NO: 10/ 081652 [\[PALM\]](#)
DATE FILED: February 21, 2002

INT-CL: [07] [G06](#) [F](#) [13/00](#)

US-CL-PUBLISHED: 710/100

US-CL-CURRENT: [710/100](#)

REPRESENTATIVE-FIGURES: 3

ABSTRACT:

A method and system transfer read data from a memory device having a data bus and a data masking pin adapted to receive a masking signal during write operations of the memory device. The method includes placing a sequence of read data words on the data bus and applying a data bus inversion signal on the data masking pin, the data bus inversion signal indicating whether the data contained each read data word has been inverted. Another method and system transfer data over a data bus. The method includes generating a sequence of data words, at least one data word including data bus inversion data. The sequence of data words is applied on the data bus and is thereafter stored. The data bus inversion data is applied to invert or not invert the data contained in the stored data words.

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File: USPT

Feb 28, 1995

US-PAT-NO: 5394366

DOCUMENT-IDENTIFIER: US 5394366 A

TITLE: Enabling data access of a unit of arbitrary number of bits of data in a
semiconductor memory

DATE-ISSUED: February 28, 1995

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Miyamoto; Takayuki	Hyogo			JP

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Mitsubishi Denki Kabushiki Kaisha	Tokyo			JP	03

APPL-NO: 07/ 925152 [PALM]

DATE FILED: August 6, 1992

FOREIGN-APPL-PRIORITY-DATA:

COUNTRY	APPL-NO	APPL-DATE
JP	3-200278	August 9, 1991

INT-CL: [06] G11 C 7/00

US-CL-ISSUED: 365/195; 365/196, 365/193, 365/189.01, 365/189.03

US-CL-CURRENT: 365/195; 365/189.01, 365/189.03, 365/193, 365/196

FIELD-OF-SEARCH: 365/195, 365/189.01, 365/196, 365/221, 365/189.02, 365/189.03,
365/189.12, 365/230.02, 365/230.09, 365/193, 364/514, 364/516

PRIOR-ART-DISCLOSED:

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	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
<input type="checkbox"/>	<u>4669064</u>	May 1987	Ishimoto	365/195
<input type="checkbox"/>	<u>4897818</u>	January 1990	Redwine et al.	365/195
<input type="checkbox"/>	<u>5313624</u>	May 1994	Harriman et al.	395/575

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"Home VTR Containing Field Memory for Correcting Crossbar and Skew Distortion in Search Mode", Nikkei Electronics, vol. 406, Oct. 20, 1986, pp. 195-214.

ART-UNIT: 251

PRIMARY-EXAMINER: LaRoche; Eugene R.

ASSISTANT-EXAMINER: Hoang; Huan

ATTY-AGENT-FIRM: Lowe, Price, LeBlanc & Becker

ABSTRACT:

A DRAM device includes a read control circuit for inhibiting read out of one or more bits of a multi-bit data output from a plurality of memory cells in response to a bit designating signal for specifying the one or more bits. By arbitrarily setting the number of bits to be output from the DRAM device and combining that output with data from one or more additional memory devices, data of an arbitrary number of bits can be generated at a high speed.

13 Claims, 17 Drawing figures

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L5: Entry 1 of 1

File: USPT

Mar 30, 2004

US-PAT-NO: 6714460

DOCUMENT-IDENTIFIER: US 6714460 B2

TITLE: System and method for multiplexing data and data masking information on a data bus of a memory device

DATE-ISSUED: March 30, 2004

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
LaBerge; Paul A.	Shoreview	MN		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Micron Technology, Inc.	Boise	ID			02

APPL-NO: 10/ 081653 [PALM]

DATE FILED: February 21, 2002

INT-CL: [07] G11 C 7/00

US-CL-ISSUED: 365/189.01; 365/195

US-CL-CURRENT: 365/189.01; 365/195

FIELD-OF-SEARCH: 365/189.01, 365/195, 365/230.06, 365/235

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	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
<input type="checkbox"/>	<u>5539430</u>	July 1996	Priem et al.	345/545
<input type="checkbox"/>	<u>5657287</u>	August 1997	McLaury et al.	365/230.01
<input type="checkbox"/>	<u>6011727</u>	January 2000	Merritt et al.	365/189.02
<input type="checkbox"/>	<u>6269103</u>	July 2001	Laturell	370/458

ART-UNIT: 2824

PRIMARY-EXAMINER: Le; Vu A.

ATTY-AGENT-FIRM: Dorsey & Whitney LLP

ABSTRACT:

A method and system masking data being written to a memory device having a data bus. One method includes applying masking data on the data bus, storing the masking data in the memory device, applying write data on the data bus, storing the write data in the memory device, and applying the stored masking data to mask the stored write data.

53 Claims, 4 Drawing figures

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US006826095B2

(12) **United States Patent**
Macri et al.

(10) Patent No.: **US 6,826,095 B2**
(45) Date of Patent: **Nov. 30, 2004**

(54) **METHOD AND APPARATUS FOR DATA INVERSION IN MEMORY DEVICE**

(56) **References Cited**

(75) Inventors: Joseph Macri, San Francisco, CA (US);
Olgo Drapkln, Richmond Hill (CA);
Grigori Temkine, Markham (CA);
Osamu Nagashima, Hamura (JP)

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5,630,106 A • 5/1997 Ishihashi 345/333
5,953,272 A • 9/1999 Powell et al. 365/201
2003/0041223 A1 • 2/2003 Yeh et al. 711/167

(73) Assignees: ATI Technologies Inc., Markham (CA);
Elpida Memory, Inc., Tokyo (JP)

* cited by examiner

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

Primary Examiner—Anh Phung
(74) Attorney, Agent, or Firm—J. D. Harriman, II; Coudert Brothers LLP

(21) Appl. No.: 10/681,014

(22) Filed: **Oct. 7, 2003**

(65) **Prior Publication Data**

US 2004-0090836 A1 May 13, 2004

Related U.S. Application Data

(63) Continuation of application No. 10/163,785, filed on Jun. 5, 2002, now Pat. No. 6,671,212.

(60) Provisional application No. 60/335,289, filed on Feb. 8, 2002.

(51) Int. Cl.⁷ G11C 16/04

(52) U.S. Cl. 365/189.07; 365/189.04

(58) Field of Search 365/189.07, 189.04,
365/189.08; 711/167, 202

ABSTRACT

A method of writing information to a synchronous memory device by examining a present word of N bits to be written, where each bit has a high or low value. The present word is compared to a previous word also having N bits to identify the number of bit transitions from a low value to a high value of vice versa. The present bit is inverted when the number of bit transitions is greater than N/2. To avoid the need for having an extra bit accompany data bytes to indicate the presence or absence of inversion, the present invention takes advantage of a data mask pin that is normally unused during writing operations to carry the inversion bit. Non-inverted data is written directly into the memory device while inverted data is first inverted again before writing to storage locations, so that true data is stored in the memory device.

29 Claims, 7 Drawing Sheets

